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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,804	03/03/2004	Takashi Takamura	118577	4351

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EXAMINER	
SEFER, AHMED N	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 07/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/790,804	TAKAMURA, TAKASHI	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3-7* is/are allowed.

6)☒ Claim(s) *1 and 2* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed April 17, 2006 has been entered; no new claims have been introduced.

Claim Objections

2. Claim 5 is objected to because of the following informalities: The recitation calling for "the gate electrode" should read "**the output gate electrode**". Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over in view of Dierickx ("Dierickx") US PG-Pub 2001/0011736, Shizukuishi USPN 6,781,178, Pain et al. ("Pain") US PG Pub 2002/0036300 and Goto ("Goto") US PG Pub 2003/0090584.

Dierickx discloses in figs. 2 and 14 a solid-state imaging device, comprising: a pixel array having a plurality of pixels (par. 0035) arranged in a matrix; and a control unit (par. 0114) that controls the pixel array; each of the pixels including: a photo diode (par. 0063) that generates carriers depending on an intensity of incident light; an accumulation region 3 that accumulates the generated carriers; an insulated-gate output transistor 7'/ 7 that outputs a signal according to a threshold voltage that changes depending on a number of the carriers

accumulated in the accumulation region; and an insulated-gate clear transistor (par. 0073) that discharges the carriers accumulated in the accumulation region, but discloses neither an insulated-gate clear transistor that discharges, during a discharging period, the carriers accumulated in the accumulation region and that discharges during an accumulation period, spilled carriers that exceed a capacity of the accumulation region nor clear transistor having a threshold and source voltage.

Shizukuishi discloses in figs. 1-4 a solid-state imaging device, comprising: a pixel array having a plurality of pixels arranged in a matrix; and an insulated-gate clear transistor WM that discharges, during a discharging period, the carriers accumulated in the accumulation region and that discharges during an accumulation period, spilled carriers that exceed a capacity of the accumulation region (col. 9, lines 51-62); and the insulated-gate clear transistor having a threshold voltage (col. 5, lines 15-23 and 54-56).

Pain discloses (figs. 1, 5 and 6, abstract and par. 0012) a solid-state imaging device, comprising: a pixel array having a plurality of pixels arranged in a matrix; and an insulated-gate clear transistor that discharges, during a discharging period, the carriers accumulated in the accumulation region and that discharges during an accumulation period, spilled carriers that exceed a capacity of the accumulation region, the accumulation period being a time period in which carriers are accumulated in the accumulation region up to the capacity of the accumulation region (par. 0042).

Goto discloses (figs. 2-5, 8-12, 34-39 and pars. 91, 97 and 177) discloses a solid-state imaging device, comprising: a pixel array having a plurality of pixels 15 arranged in a matrix; and an insulated-gate clear transistor 9N/9P/15b that discharges, during a discharging period, the

carriers accumulated in the accumulation region and that discharges during an accumulation period, spilled carriers that exceed a capacity of the accumulation region, the accumulation period being a time period in which carriers are accumulated in the accumulation region up to the capacity of the accumulation region and the insulated-gate clear transistor having a threshold voltage and a source voltage, the source voltage indicative of a number of carriers accumulated in the accumulation period, a control unit 19 setting the transistor to an "on" state when the source voltage exceeds the sum of the predetermined voltage and the threshold voltage (pars. 80, 108 and 182).

Since Dierickx, Pain, Goto and Shizukuishi are all from the same field of endeavor, solid-state imaging devices, Goto's, Pain's and Shizukuishi's teachings would have been recognized in the pertinent art of Dierickx. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate an insulated-gate clear transistor with Dierickx's device, since that would improve sensitivity and response speed as taught by Shizukuishi. It would have been obvious to incorporate Pain's teachings so as to obtain low noise and low image lag as taught by Pain. It would have been obvious to incorporate Goto's teachings to prevent noise from being generated as taught by Goto

As for the recited operational limitations of the control unit and the clear transistor, claims directed to an apparatus must distinguish from the prior art in terms of structure rather than function, In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997); See also In re Swinehart, 439 F.2d210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971; see also In re Danly, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959).

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dierickx in view of Shizukuishi, Pain and Goto.

Dierickx discloses in figs. 2 and 14 a solid-state imaging device, comprising: a pixel array having a plurality of pixels (par. 0035) arranged in a matrix; and a control unit (par. 0114) that controls the pixel array; each of the pixels including: a photo diode (par. 0063) that generates carriers depending on an intensity of incident light; an accumulation region 3 that accumulates the generated carriers; an insulated-gate output transistor 7'/ 7 that outputs a signal according to a threshold voltage that changes depending on a number of the carriers accumulated in the accumulation region; and an insulated-gate clear transistor (par. 0073) that discharges the carriers accumulated in the accumulation region, but discloses neither an insulated-gate clear transistor that discharges spilled carriers in order to prevent carriers from entering the accumulation region nor clear transistor having a threshold and source voltage.

Shizukuishi discloses in figs. 1-4 a solid-state imaging device, comprising: a pixel array having a plurality of pixels arranged in a matrix; and an insulated-gate clear transistor that discharges spilled carriers in order to prevent carriers from entering the accumulation region (col. 9, lines 51-62); and the substrate region comprising: an upper region 23 (horizontal portion of layer 23) that is formed in a vicinity of the gate electrode of the clear transistor and that has a relatively low impurity concentration; and a lower region 25 that is formed below the upper region and that has a relatively high impurity concentration.

Pain discloses (figs. 1, 5 and 6, abstract and par. 0012) a solid-state imaging device, comprising: a pixel array having a plurality of pixels arranged in a matrix; and an insulated-gate clear transistor that discharges, during a discharging period, the carriers accumulated in

the accumulation region and that discharges during an accumulation period, spilled carriers that exceed a capacity of the accumulation region, the accumulation period being a time period in which carriers are accumulated in the accumulation region up to the capacity of the accumulation region (par. 0042).

Goto discloses (figs. 2-5, 8-12, 34-39 and pars. 91, 97 and 177) discloses a solid-state imaging device, comprising: a pixel array having a plurality of pixels 15 arranged in a matrix; and an insulated-gate clear transistor 9N/9P/15b that discharges, during a discharging period, the carriers accumulated in the accumulation region and that discharges during an accumulation period, spilled carriers that exceed a capacity of the accumulation region, the accumulation period being a time period in which carriers are accumulated in the accumulation region up to the capacity of the accumulation region and the insulated-gate clear transistor having a threshold voltage and a source voltage, the source voltage indicative of a number of carriers accumulated in the accumulation period, a control unit 19 setting the transistor to an "on" state when the source voltage exceeds the sum of the predetermined voltage and the threshold voltage (pars. 80, 108 and 182).

Since Dierickx, Pain, Goto and Shizukuishi are all from the same field of endeavor, solid-state imaging devices, Goto's, Pain's and Shizukuishi's teachings would have been recognized in the pertinent art of Dierickx. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate an insulated-gate clear transistor with Dierickx's device, since that would improve sensitivity and response speed as taught by Shizukuishi. It would have been obvious to incorporate Pain's teachings so as to obtain low noise and low

image lag as taught by Pain. It would have been obvious to incorporate Goto's teachings to prevent noise from being generated as taught by Goto.

As for the recited operational limitations of the control unit and the clear transistor, claims directed to an apparatus must distinguish from the prior art in terms of structure rather than function, In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997); See also In re Swinehart, 439 F.2d210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971; see also In re Danly, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959).

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dierickx in view of Shizukuishi, Takayama and Goto.

Dierickx discloses in figs. 2 and 14 a solid-state imaging device, comprising: a pixel array having a plurality of pixels (par. 0035) arranged in a matrix; and a control unit (par. 0114) that controls the pixel array; each of the pixels including: a photo diode (par. 0063) that generates carriers depending on an intensity of incident light; an accumulation region 3 that accumulates the generated carriers; an insulated-gate output transistor 7'/ 7 that outputs a signal according to a threshold voltage that changes depending on a number of the carriers accumulated in the accumulation region; and an insulated-gate clear transistor (par. 0073) that discharges the carriers accumulated in the accumulation region, but discloses neither an insulated-gate clear transistor that discharges spilled carriers in order to prevent carriers from entering the accumulation region nor clear transistor having a threshold and source voltage.

Shizukuishi discloses in figs. 1-4 a solid-state imaging device, comprising: a pixel array having a plurality of pixels arranged in a matrix; and an insulated-gate clear transistor that discharges spilled carriers in order to prevent carriers from entering the accumulation region (col.

9, lines 51-62); and the substrate region comprising: an upper region 23 (horizontal portion of layer 23) that is formed in a vicinity of the gate electrode of the clear transistor and that has a relatively low impurity concentration; and a lower region 25 that is formed below the upper region and that has a relatively high impurity concentration.

Takayama discloses (figs. 1-9 and 19, abstract and par. 0161) a solid-state imaging device, comprising: a pixel array 50 having a plurality of pixels arranged in a matrix; and an insulated-gate clear transistor Q2 that discharges, during a discharging period, the carriers accumulated in the accumulation region and that discharges during an accumulation period, spilled carriers that exceed a capacity of the accumulation region, the accumulation period being a time period in which carriers are accumulated in the accumulation region up to the capacity of the accumulation region.

Goto discloses (figs. 2-5, 8-12, 34-39 and pars. 91, 97 and 177) discloses a solid-state imaging device, comprising: a pixel array having a plurality of pixels 15 arranged in a matrix; and an insulated-gate clear transistor 9N/9P/15b that discharges, during a discharging period, the carriers accumulated in the accumulation region and that discharges during an accumulation period, spilled carriers that exceed a capacity of the accumulation region, the accumulation period being a time period in which carriers are accumulated in the accumulation region up to the capacity of the accumulation region and the insulated-gate clear transistor having a threshold voltage and a source voltage, the source voltage indicative of a number of carriers accumulated in the accumulation period, a control unit 19 setting the transistor to an "on" state when the source voltage exceeds the sum of the predetermined voltage and the threshold voltage (pars. 80, 108 and 182).

Since Dierickx, Takayama, Goto and Shizukuishi are all from the same field of endeavor, solid-state imaging devices, Goto's, Takayama's and Shizukuishi's teachings would have been recognized in the pertinent art of Dierickx. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate an insulated-gate clear transistor with Dierickx's device, since that would improve sensitivity and response speed as taught by Shizukuishi. It would have been obvious to incorporate Takayama's teachings since that would reduce power consumption as taught by Takayama. It would have been obvious to incorporate Goto's teachings to prevent noise from being generated as taught by Goto.

As for the recited operational limitations of the control unit and the clear transistor, claims directed to an apparatus must distinguish from the prior art in terms of structure rather than function, In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997); See also In re Swinehart, 439 F.2d210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971; see also In re Danly, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANS
June 21, 2006